Reduction in Power of Logic Circuits using Device Stacking and Virtual Power Rails

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Abstract -This paper discusses energy-saving measures for reducing power. With the introduction of Deep Sub-Micron (DSM) technology, which allows for more complicated operations to be combined into a single chip, rapid advancements in semiconductor technology have resulted in smaller transistor feature sizes. The battery-powered technology forms the spine of the growing industry for portable mobile phones utilised globally today. To increase battery life, similar mobile devices such as book computers, personal communication resources (cell phones, pocket PCs, PDAs), hearing aids, and implanted pacemakers must have a larger calculator capacity. One of the biggest technical issues for DSM in the building of the CMOS circuit is power utilisation.

This study presents extensive investigation and analysis of two energy reduction techniques described in this paper on the innovative reduction approach. EDA Tanner imitates using 16nm CMOS technology. A voltage of 0.5V is used to power the circuits. Reduce static power without interfering greatly with the utilisation of alternating electricity.

Index Terms - Power and Clock gating, retention, transistor stacking.

I. INTRODUCTION

In the deep submicron range, technical measurement results in subthreshold . There is a need for effective current reduction methods. This paper provides fundamental gate circuits as well as a low-power adder circuit. This considerable reduction is accomplished by disconnecting sense cells from the ground and feeding rails via a power-cutting mechanism. The input approach decreases static power utilisation but increases the latency of sensible cells in deep submicron CMOS circuits, resulting in significantly reduced performance. To boost performance, more transistors are added to the circuit, reducing the usage of flexible and high .

In CMOS circuits, power dissipation is divided into two portions. Strong scattering can be induced by charging and discharging of the load, such as gate switching, or current "short circuit" when both the PMOS and NMOS stacks are partly open, but weak scattering can be caused by sub-threshold from transistors that are turned off. junction from the source / discharge fluid, and current resistance in measured circuits Power utilisation may be reduced in active, standby, and sleep modes. While the chip is in operation, active power is applied. Instinct frequently rules flexibility [8].

To reduce , the provision for unneeded circuits is switched off in sleep mode[8]. This considerably decreases the necessary sleep capacity, but the chip requires time and energy to wake up, thus sleep can only function if the chip does nothing for a long enough period of time. There are several potential solutions for lowering energy and energy utilisation. The measurement of voltage supply (Vdd) is regarded as one of the most effective in the system for reducing power utilisation in CMOS circuits. Threshold Voltage (Vth) has also been decreased to maintain the needed current drive. When the threshold voltage Vth is reduced, the capacity increases significantly. Technical measures are typically used to minimise the Vdd / Vth rating in order to maintain capacity under control.. Power gating is another possibility [2]. While the chip is in sleep mode, the power supply and bottom line are disconnected from the circuit block.

II. RELATED WORK

Ankita Nagar proposed a reduction in power dissipation at base gates using transistor stacking. It was found that when the low input value increases in the NAND gate position the power dissipation decreases and in NOR the power output of the gate decreases with the increase of the input voltage vector combination. Jatin Mistry, James Myers and Basher introduced a method called sub clock power gating. Amit Bakshi offers the idea of reducing low power and low-pitched noise during sleep to a functional mode change. Shota Ishihara, Masanori Hariyama offers a breakdown of the input method such as a good grain power gating and a grain power gate. In the coarse grain gating one sleep transistor is assigned to all components and in finegrain power gating each component will have sleep transistors. To reduce subthreshold in sleep mode Seta et al use distorted body bias in deep submicron circuits. The proposed T Kuroda et al CMOS flexible uses TWIN technology well or triple. An additional cycle of using foot bias was proposed by Kawaguchi et al and this procedure is called super cut off CMOS power gating. Discharge of large cores is possible by using multiple switch modes. . In this paper we have proposed

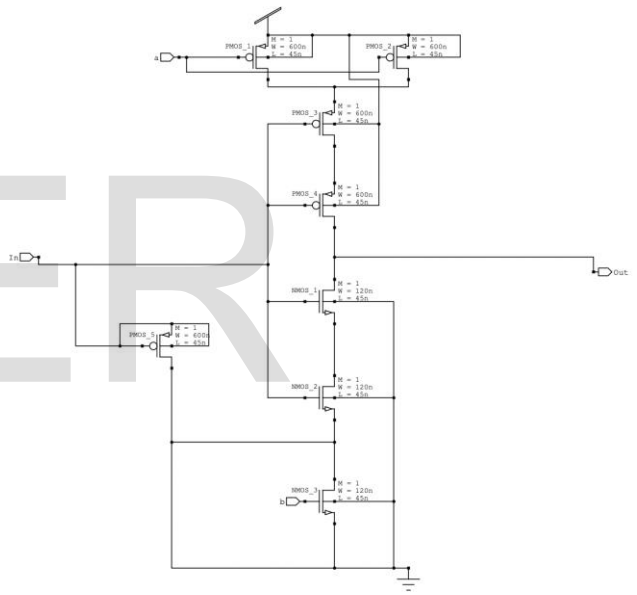
a design to reduce energy utilisation using an energy gate with reverse body bias and additional devices to improveits application.

III. Design Methodology

The majority of power outages in CMOS circuits are caused by a logical change that fluctuates with the supply voltage. Significant power loss reductions can thus be realised by running at a lower supply voltage.

The sleep transistor is the primary user of the gating circuitry's power output. It is critical to ensure that the waiting power saved by employing the power input technique is more than the power utilised by the power gating circuit. The two basic steps in energy conservation are coarse grain gating and fine grain power gating. The first form, coarse grain gating, assigns a single sleep transistor to a greater number of circuits. Sleep transistors used to take up less space and power. If one of the circuits inside this character is active, all circuits that share the same sleep transistor cannot be put to sleep. Instead, in the second kind, fine grain power gating, each circuit has its own sleep transistor, so that if any circuit fails, the same circuit may be put to sleep promptly. As a result, the number of sleep transistors in the grain energy field is significantly larger than in the coarse grains. Because the grain power gate effectively cuts off most of the dynamic and stationary power, such approaches are employed when dynamic or stationary force is a significant issue. To reduce current , the sleep transistor threshold voltage should be increased[3]. As a result, high threshold transistors are used as sleep transistors. It is also important to keep in mind that the width of the receiving sleep transistor should be smaller than the overall width of the transistors in the pull-down circuit. However, as compared to the coarse grain input technique, the surface area of the ideal grain input method grows as the number of sleep transistors increases.

Power gating is one method for reducing power. As slow-moving sleep transistors, power input use PMOS or NMOS. The power gate involves shutting off the power when in standby mode and turning it back on if required. High Vth transistors are used as switches to cut off the power and are situated between the block power and low pins and rails. Between the power pins and the power rails is a PMOS transistor head switch. An NMOS transistor positioned between the base pins and ground rails serves as a foot switch. As a result, the controlled block is now powered by virtual power rail rather than high power rail (always rows). A power or sleep signal is used to control power switches. The power signal requires a suitable amount of 1 to switch off the power for a title change. The reverse occurs with a foot change. As crucial as energy conversion is the best technique to distribute and supply energy throughout the project. The power network should be designed to minimise power interruptions while still adequately supplying all typical blocks and cells under development. A state maintenance technique can also be utilised. You may be necessary to store the block state depending on the request. As a result, when the power is switched on and off, the block can revert to its original functioning condition. This is accomplished by employing state maintenance transistors. Separating the output signals from the blocked blocks may also be required. When these signals are floating, they can draw current to a neighbouring block, which represents input signals. When more than one transistor in the stack is turned off, the current of the sub-threshold flowing through a series of transistors connected to the series diminishes. This is referred to as the stacking effect. Also referred to as self-reverse bias. currents on NMOS or PMOS transistors rely heavily on the four terminals of transistors . The VG gate voltage is “0” and this will increase the Vs source voltage of the NMOS transistor. This



reduces the current sub-threshold with growth [7][8]. In our design we consider transistor overload, retention transistor and the hybrid process of the energy reduction reduction.

IV. Proposed Work

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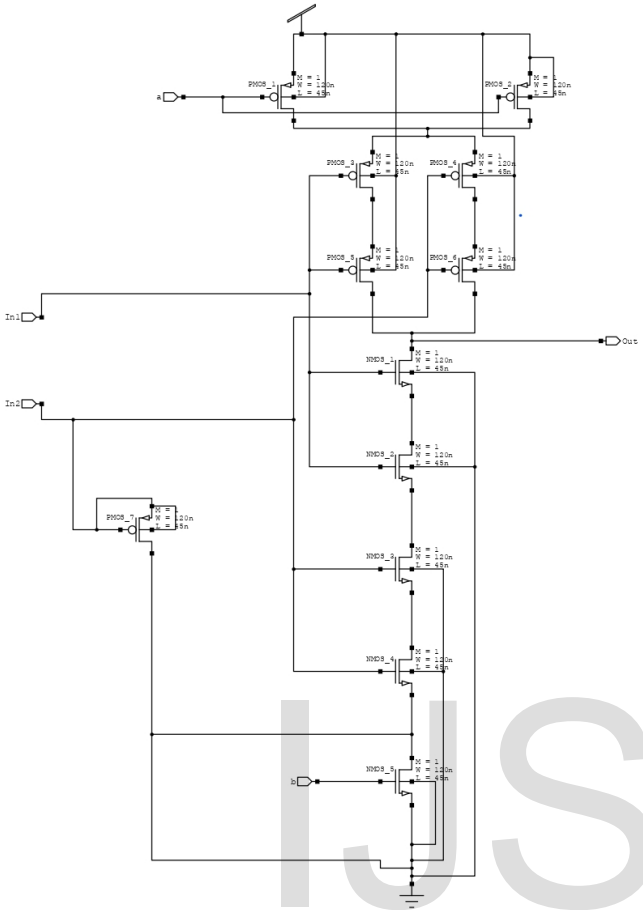

Fig 1. NOT Gate with Stacking transistor and Power Gating Applied

DESIGNED NOT GATE

The circuit in this case is made up of the retention transistors depicted in Fig 1. A symmetric virtual clamping rail system is applied in this case. This application operates by lowering the voltage supply to Vth rather than totally shutting down as in traditional Power Gating[2]. To produce a lower voltage, symmetrical virtual rail clamping is applied. In this scenario, NMOS pairs and PMOS transistors are employed in the power gate concept's head and foot. The high-end NMOS_2 transistor is connected in the pull network with the more threshold PMOS transistors P0 and P1, and the higher threshold PMOS transistor PMOS_4 is connected in the pull network with the greater threshold NMOS transistor NMOS_1.

DESIGNED NAND GATE

Fig 2. Designed NAND Gate with Virtual Power Rails.

An extra device, a high voltage threshold PMOS_PMOS_6 can be used to alter the outflow of a stcking NAND circuit. As illustrated in Fig. 2, the PMOS transistor PMOS_6, its gate, and its source are coupled together, and any input is delivered to the gate / source, which is subsequently connected to both the ground and the virtual ground. This extra High Voltage Threshold transistor helps to reduce dynamic and maximum power utilisation while maintaining circuit performance. If either of the inputs is low, the output of a CMOS NAND gate is high. In the alternative, if both inputs are High, the output is Low. Furthermore, distorted body bias and Stacking transistorprocedures [4] are utilised to limit the possibility of . I pMOS sleep and nMOSsleep are set to Low and High, respectively, in the active mode, while sleep transistors P0, P1, and NMOS_4 are switched on. Because these sleep-resistant IN-ON transitors are tiny, the virtual railroads function similarly to a genuine power rail. If both output headers are low, this means that all PMOS transistors in the PNT network are closed and all NMOS transistors (NMOS_0, NMOS_1, NMOS_2, and NMOS_3) in the drain network are OPEN and flowing continuously down. The NMOS transistor NMOS_4 also reduces dynamic energy usage. Similarly, when both inputs are OPEN, all NMOS transistors in the downtime network are OPEN, and current flows through the High Voltage Threshold PMOS transistor PMOS_6 as OPEN, reducing power utilisation [3].

When INMOS_1 and INMOS_2 are higher and lower, the output is higher because PMOS transistors PMOS_2 and

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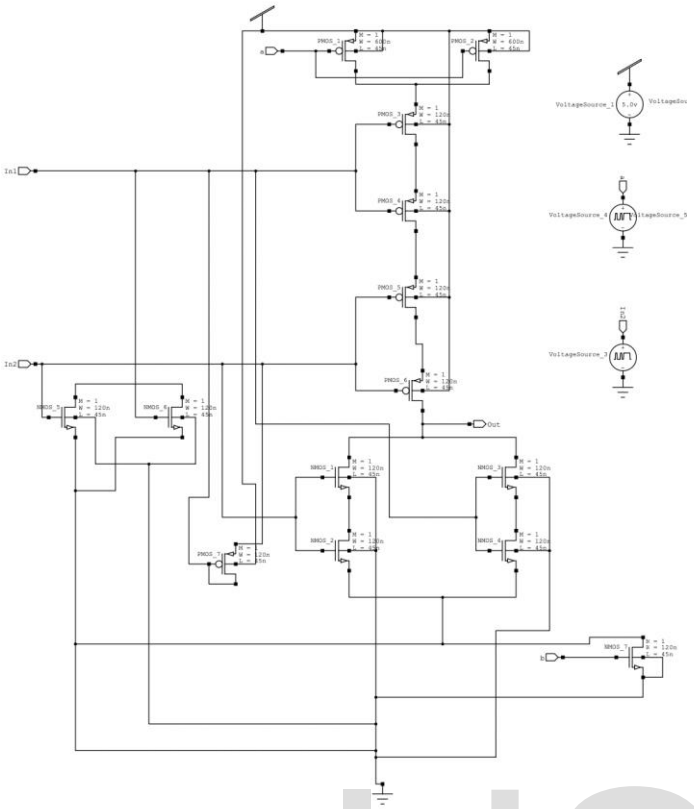

PMOS_4 are open and High Voltage Threshold PMOS transistor PMOS_6 is open, and NMOS transistors (NMOS_2 and NMOS_3) are now flowing following input via PMOS PMOS_6. As a result, the dynamic energy is reduced. When the INMOS_1 and INMOS_2 inputs are low and high, respectively, PMOS_PMOS_6 closes and the output is high because transistors PMOS_3 and P5 are turned on and NMOS_2 and NMOS_3 and current leaks pass into NMOS Transistor NMOS_0 and NMOS_1 flows to Gnd through biassing (Reverse Body). The power switch decreases power in standby mode by employing pMOSsleep and nMOSsleep.IThe pMOSsleep and nMOSsleep registers are set to Up and Down, respectively, in standby mode, and the sleep transistors are closed, isolating the NAND gate circuit from the power and ground lines. This technique reduces the circuit's capacity and flexible power utilisation significantly, but it also increases the circuit's size and latency.

High Voltage Threshold NMOS transistors are smaller in size than High Voltage Threshold PMOS transistors. When more than one transistor is isolated from the stack, employing transistor accumulation in the NAND gate circuit improves resistance and significantly reduces sub threshold current travelling through a large number of connected transistors. Here due to the overlap effect [6], the current of the subthreshold by a sensible gate depends on the conditions of the main input. But the flexibility of this circuit is increasing as more and more transistors are used in this circuit.

DESIGNED NOR GATE

As illustrated in Fig 3, two high voltage NMOS transistors NMOS_0 and NMOS_1 are linked in this circuit. and their sources are linked in the virtual VGND, and another high voltage PMOS PMOS_6 is connected to the gate and drain tied, as well as its source. on Vdd virtual supply [5]. This method employs transistor stacking. This procedure contributes to a considerable reduction in capacity. NOR gate output is normally low when the other input is high and high when both inputs are low. The resistance between the electric

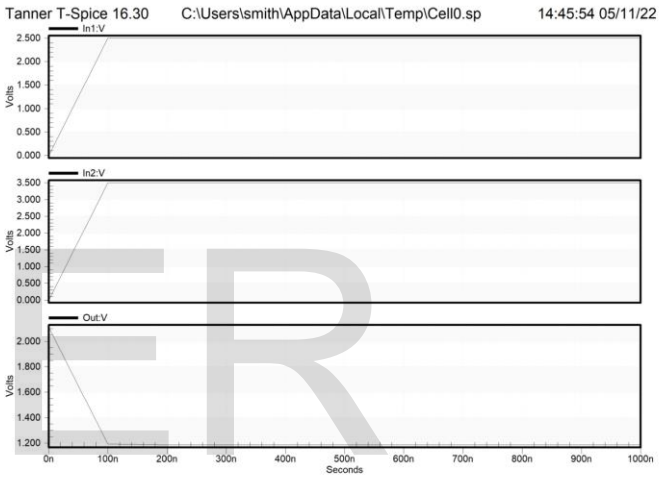

Fig 3. Designed NOR Gate with Virtual Sleep Awake Power Rails.

Current and the real ground grows throughout this Stacking transistorprocess [4], reducing a considerable amount of energy. High threshold voltage transistors are added to the Stacking transistorlogic circuit..

When compared to the simple power output technique, power output is higher. Furthermore, the supply voltage is decreased to 0.5V, resulting in a significant reduction in active power and put aside. When both inputs are high in dynamic mode, these two High Voltage Threshold NMOS NMOS_0 and NMOS_1 are ON, as are all NMOS transistors in the logic circuit. NMOS_4 and N6 are responses to inputs using these High Voltage Threshold NMOS transistors NMOS_0 and NMOS_1, reducing dynamic energy usage. When the INMOS_1 input is low, the logic circuit's transistors PMOS_2 and PMOS_3, which are linked to the Vdd, switch on, and the same input is placed into the High Voltage Threshold PMOS transistor PMOS_6.This turns on the High Voltage Threshold PMOS_PMOS_6 with its source connected to the Vdd, and tries

to boost the output to the top. When the INMOS_2 input is high, the PMOS PMOS_4 and P5 transistors shut, causing the output to be pulled LOW. If the other INMOS_2 input is also low, the PMOS transistors PMOS_4 and P5 are turned on, causing the output to be pushed higher. If INMOS_1 is high and INMOS_2 is low, PMOS PMOS_2 and PMOS_3, as well as the high threshold voltage PMOS_PMOS_6 are turned off, and PMOS transistors PMOS_4 and P5 are turned on.

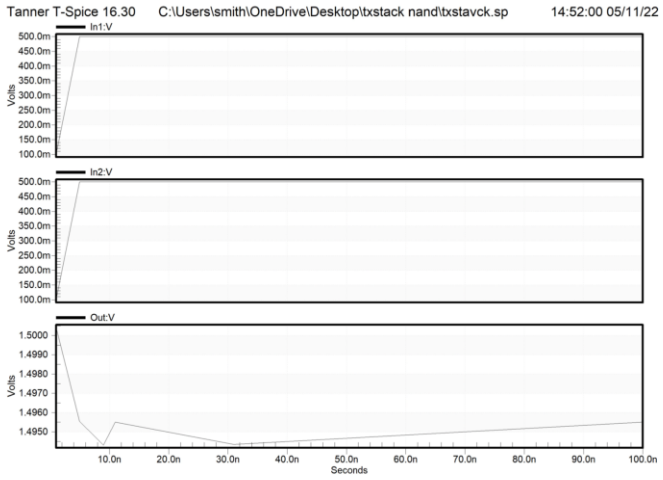

Fig 4. Designed Virtual Power Rails NOT Gate Waveform

IV. Simulation

All the Designs are Drawn and Simulated on EDA Tanner Tool Environment using 16nm latest cutting edge Technology
The power is measured in 3 modes Max. Power, Min power, and Average Power but readings are considered for Average Power only at 100ns Step time in Transient Analysis
All Supply Voltages are kept to 1.5v and Input Voltages at 0.5v

	Standard NOT Gate	Des
FETS	2	8
Sources	2	4
nt Nodes	9	36
Nodes	12	41
ower	4.884596e-007 watts	2.356527e-007 watts

TABLE I.

Table I. Summarises comparision in simulated results for Standard NOT Gate and Designed NOT Gate highlighting Average Consumed Power.

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TABLE II.

	Standard NAND Gat
MOSFETS	4
Voltage Sources	3
Independent Nodes	18
Total Nodes	22
Avg Power	1.288522e-004 watts

Table II. Summarises comparision in simulated results for Standard NAND Gate and Designed NAND Gate highlighting Average Consumed Power.
Fig 5. NAND Gate Waveform

TABLE III.

	Standard NOR Ga
MOSFETS	4
Voltage Sources	3
Independent Nodes	18
Total Nodes	22
Avg Power	9.10625e-006wat

Table III. Depicts comparision between Conventional NOR Gate Consumed Power vs Designed NOR Gate Power.

V. Conclusion

One of the most efficient methods to save energy is to measure it. The method enables many CMOS circuits to run in a sub-0.5V discharge supply area with very low power utilisation. We also use energy extraction strategies to limit

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capacity. Multiple power gating in hybrid mode decreases static power, latency, and output power delay.

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